Implementation of the Turbo-TCM and Space-Time Code Modulation with FPGA in Transceiver

快速格子狀編碼調變及時空編碼調變使用 FPGA 之設計與實現

Abstract

The presence of Turbo-TCM and Space-Time code modulation constitutes a major channel coding in transceiver. We have designed and simulated CODE by Altera in software, then can be improved by FPGA. We also use turbo coding to increase bandwidth efficiency and BAHL and Viterbi decoding enhance performance. In this paper, the Turbo-TCM and Space-Time code modulation concatenation can improve decoding speed and enhance coding gain relatively by without increasing bandwidth in the wireless communication system. We get very good performance target FPGA with two receive antennas that can be increased power gain with an 8 state 8-PSK for the concatenation of TTCM and STBC.

摘要

我們針對實用性加速格子狀編碼調變 (Turbo Coded Pragmatic Trellis Coded Modulation,TCPTCM),使用 FPGA 設計編解碼單元 (encoder unit and decoder unit ,CODEC) 模擬編解碼過程,我們選擇使用 8-PSK 的調變技術,且使用加速編碼方式以增加頻寬效益,解碼使用 BAHL 和 Viterbi 解碼器以增加解碼的準確性。在本篇報告中 TCPTCM 在不增加頻寬下,可改善無線通訊系統中傳送及解碼速度及相對提高碼增益(coding gain)。

Keyword

STTC (Space-Time Trellis code), TTCM (Turbo-TCM), STBC (Space-Time Block Codes), STCM (Space-Time coded modulation), MAP(maximum a posteriori probability)

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Abstract

The presence of Turbo-TCM and Space-Time code modulation constitutes a major channel coding in transceiver. We have designed and simulated CODE by Altera in software, then can be improved by FPGA. We also use turbo coding to increase bandwidth efficiency and BAHL and Viterbi decoding enhance performance. In this paper, the Turbo-TCM and Space-Time code modulation concatenation can improve decoding speed and enhance coding gain relatively by without increasing bandwidth in the wireless communication system. We get very good performance target FPGA with two receive antennas that can be increased power gain with an 8 state 8-PSK for the concatenation of TTCM and STBC.

1. Introduction

The efficiency and reliance of the data transmission are contradictory in digital communication system. It would be meaningful to study and solve that the bit error rate raises causing by increased at as data rate in communication system design and implementation in general. Berrou et al.[1] invented turbo codes. Rate-1/2 turbo code with BPSK modulation in AWGN channel simulated and showed coding gain up to 11 dB which was within 0.5dB of the Shannon capacity limit. Stefanov and Duman[2] showed that turbo coded modulation scheme using the QPSK constellation outperforms the space-time block and trellis codes significantly. They observed very high gains over the corresponding space-time codes for large interleaver lengths, which is suitable for data communication. Bruce and Calvin[3] invented turbo code being applied in pragmatic trellis-coded modulation (PTCM). The signal constellation mapping 8-PSK they made the obvious substitution of a rate-1/3 turbo encoder comprising two identical rate-1/2 recursive systematic convolutional codes which are concatenated in parallel and separated by an interleaver. Gozali and Woerner[4] designed with the use of multiple transmit antennas for improving the data rate and/or reliability of wireless communication, they called the Space-Time Trellis code(STTC).

Hammons and Gamal[5] have developed general design criteria for PSK-modulated space-time codes, based on the binary rank of the unmodulated codwords, to ensure that full spatial diversity is achieved. Naguib et al.[6] proposed a new advanced modem technology based on the use of concatenated space-time coded modulation (STCM) with multiple transmit and/or multiple receive antennas for high data rate wireless communication. A detailed design for a narrowband TDMA/STCM based modem is also presented. Bauch and Naguib[7] addressed the equalization problem for communication system employing space-time coding with multiple transmit antennas. They derived a symbol-by-symbol MAP equalizer/decoder for space-time coded signals over frequency selective channels. Liu et al.[8] used the maximum a posteriori probability(MAP) algorithm as a trellis-based MAP decoding algorithm. Using the structural of sectionalized trellis for linear block codes, the decoding complexity and delay of the MAP algorithm can be reduced. It is the turbo decoding that achieves an error performance near the Shannon limit. Seshadri et al. [9] proposed a new advanced modem technology based on the use of concatenated Space-Time coded modulation(STCM) with multiple transmit and/or multiple receive antennas for high data rate wireless communication. Gerhard[10] invented for high data rate transmission over wireless fading channels concatenation the Turbo-TCM(TTCM) and Space-Time Block Codes(STBC) which provided the maximal possible diversity advantage for multiple transmit antenna systems with a simple decoding algorithm.

In this paper, we have been implementation of the Turbo-TCM and Space-Time code modulation with FPGA and description the STBC system, and derive a soft output symbol by symbol MAP decoding rule. We design that the generation matrix is orthogonal in encoder with diversity technology and then it can reduce the multipath interference. To simplify our study, we use FPGA as simulation to design CODEC in concatenation TTCM and STBC to improve channel coding generation bits and error correction required decoding transmission speed: besides, it increased coding gain and performance by power without increasing transmitted bandwidth and required it by power. Therefore, TTCM and STBC would be very helpful in high speed and massive data transmission. In Section 2, we will introduce STBC encoder and decoder system model. Implementation of the CODEC of the concatenation Turbo-TCM and Space-Time code system hardware is in Section 3. In Section 4, computer simulation results are presented to show the circuit diagram and the conclusions are addressed in Section 5.

2. Modeling of the CODEC

The STBC encoder block diagram[10] for which C_1, . . . , C_K are the binary source

signal. We can let **c**=(C_1, . . . , C_K) to denote the sequence of real valued symbols ($C_i \in$ {0, 1, . . . , M-1}) with the mapping M-PSK(M=8) on complex constellation symbols x_i, i=1,2, . . . ,K. The K-th block of the complex symbols are x_i and (p * n_T). We also have the p is the encoder producing the mapping bits and the n_T is expressed diversity antennas. Then, we assume p=2, n_T=2 and K=2 as:

$$\mathbf{G}=\begin{bmatrix} g_{11} & \cdots & \cdots & g_{1n_T} \\ \vdots & \cdots & \cdots & \vdots \\ \vdots & \cdots & \cdots & \vdots \\ g_{p1} & \cdots & \cdots & g_{pn_T} \end{bmatrix} \quad \mathbf{G}=\begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix}=\begin{bmatrix} x_1 & x_2 \\ -x_2^{*} & x_1^{*} \end{bmatrix}$$

Where **G** matrix is achieve orthogonal in encoder with diversity technology and then it can reduce the multipath interference. Thus the signal $\gamma_j(t)$ arriving at the front end of receiver j is given by

$$\gamma_j = \sum_{i=1}^{n_T} \alpha_{i,j} C_i + \eta_j \qquad (1)$$

Where the $\alpha_{i,j}$ as the complex fading gain from the j-th transmitter antenna to the i-th receiver antenna, for $\alpha_{i,j}$ ~N(0,1) is assumed to be a zero-mean circularly symmetric complex Gaussian random variable with unit variance. It is also assumed that the fading gains remain constant over an entire signal frame, but they may vary from one frame to another. The symbol stream C_i is partitioned into blocks, with each block consisting of n_T symbols. Due to the existence of the interleaver, we are ignore the temporal constraint induced by the outer convolutional encoder and assumed that the set **c** contains independent symbols. From the STBC decoder, we only need to consider one block of symbols in the code symbol stream. It is further assumed that the symbol streams of all users are mutually independent and η_j is an additive white Gaussian noise(AWGN) channel which assume that the channel noise is processed with two-side spectrum density $N_o/2$. Let us further assume the codes with Gaussian and zero mean, therefore, we use Baye's rule that the transmitted sequence **c** is given the received sequence **r**=(r_1, . . . , r_p) and the maximum a posteriori probability can be expressed as[10]:

$$P(c_1,\ldots,c_K/r_1,...,r_p) = \frac{P(r_1,\ldots,r_P/c_1,\ldots,c_K)P(c_1,...,c_K)}{P(r_1,...,r_P)} \qquad (2)$$

Where $P(r_1,\ldots,r_P/c_1,\ldots,c_K)=\left(\frac{1}{\sqrt{2\pi\cdot\frac{N_o}{2}}}\right)^N e^{-\frac{1}{2\sigma^2}\sum_{j=1}^{n_R}\sum_{t=1}^{P}\left|r_j(t)-\sum_{i=1}^{n_T}g_{ti}\alpha_{ij}\right|^2}$ (3)

for $\left(\frac{1}{\sqrt{2\pi\cdot\frac{N_o}{2}}}\right)^N$ is constant with N-way; t=1,…,p is function of time; and each of j=1,…,n_R is the receive of antennas. Then, we can get the $\gamma_j(t)$ of the signals transmitted from the n_T antennas as:

$$P(c_1,\ldots,c_K)=\prod_{i=1}^{K}P(c_i) \qquad (4)$$

Where the c_i are mutually independent random variables. Substituting Eq.(3) and Eq.(4) into Eq.(2), and taking the natural logarithm, we have

$$\begin{aligned}&\ln P(c_1,\ldots,c_K/r_1,\ldots,r_P)\\&=\text{constant}\\&\frac{1}{2\sigma^2}\left\{\left(\sum_{j=1}^{n_R}\left(\sum_{t=1}^{P}\left[-r_j(t)\sum_{i=1}^{n_T}g_{ti}^{*}\alpha_{ij}^{*}\right.\right.\right.\right.\\&\left.\left.\left.\left.-r_j^{*}(t)\sum_{i=1}^{n_T}g_{ti}\alpha_{ij}\right]+\sum_{t=1}^{p}\sum_{i=1}^{n_T}\left|\alpha_{ij}\right|^2\left|g_{tj}\right|^2\right)\right\}\\&+\ln\prod_{i=1}^{K}P(c_i)\end{aligned}$$

(5)

Which the g_{ti} in one column of **G** are transmitted from the same antenna and therefore are multipled with the same fading factor α_{ij} and since the columns in **G** are orthogonal. (*) conjugate operation in complex. Using the MAP decoding rule, we can get

$$\max\{P(c_1,\ldots,c_K/r_1,\ldots,r_P)\}$$

$$
\begin{aligned}
&= \max \\
&\left\{ \sum_{j=1}^{n_R} \left(\sum_{t=1}^{P} \left[r_j(t) \sum_{i=1}^{n_T} g_{ti}^{*} \alpha_{ij}^{*} \right. \right. \right. \\
&\left. \left. \left. + r_j^{*}(t) \sum_{t=1}^{n_T} g_{ti}^{*} \alpha_{ij} \right] - \sum_{t=1}^{P} \sum_{i=1}^{n_T} \left| \alpha_{ij} \right|^2 \left| g_{tj} \right|^2 \right) \right\} \\
&+ \vec{b}_i
\end{aligned}
\tag{6}
$$

Where $\vec{b}_i = 2\sigma^2 \ln \prod_{i=1}^{K} P(c_i)$ and each entry g_{ti} of **G** corresponds to a certain symbol c_i. In Eq.(6), $r_j(t)$ is the receive sequence at t; g_{ti} is each entry of **G** corresponds to a certain symbol c_i and g_{ti}^{*} is each entry of **G** corresponds to a certain complex symbol c_i. We have $\max\{P(c_1,\ldots,c_K/r_1,\ldots,r_P)\} = \vec{b}_i$ if noise interference of fading factor α_{ij} is zero. We can get the model of the receive sequence, and when arriving at the receiver, the receive sequence $r_j(t)$ are first passes an operation to get (d_1, . . . , d_i), then select the maximum possible receive sequence be return initially binary sequence.

3. FPGA implementation of the CODEC

A. Description of the CODEC

The block diagram of concatenation Turbo-TCM and Space-Time code system are shown in Fig.1. We use two identical rate 1/2 Turbo-Code RSC (Recursive Systematic Convolutional) and an interleaver [2]. A binary rate 1/2 RSC code is obtained from a NSC (Non Systematic Convolutional) code by using a feedback loop. The block diagram is rate 1/2 RSC, including interleaver is shown in Fig.2. In this paper, we use Turbo-Code 4bits/Hz using 8-PSK 8state and select p=2, n_T=2. Note that MAP, Viterbi algorithm and modified BAHL et. algorithm decoder are considered in decoder design. Concatenation Space-Time code and TTCM, we have the decoder algorithm with the modification of BAHL et. We can use preload unit to go by decoder resolve into the input sequence signal. The p steps which is decoding steps is more increase and the decoder more accuracy. The implementation of the encoder and decoder are described in later respectively.

B. Implementation of the Encoder

A rate 1/3 turbo encoder comprising two identical rate 1/2 RSC which are concatenated in parallel and separated by an interleaver. The rate 1/2 RSC is obtained an XOR (Exclusive OR) gate and 1-bits D type Flip-Flop. The encoder unit of the CODEC are comprised both rate 1/3 turbo encoders. The input bit and output bit of a

rate 1/3 turbo encoder are 2 and 5. We use a NOT gate and multiplexer to get an interleaver. Then, the output sequence of the encoder passes two of 5-bits D type Flip-Flop.

C. Implementation of the Decoder

The algorithm minimizes the bit error probability in decoding linear block and convolutional codes and yields the APP(A Posteriori Probability) for each decoded it. We have the decoder unit taken by MAP decoder algorithm and comprise four preload units and four MAP units. The preload unit and MAP unit are described in later.

(I) Preload Unit

We select the 5-bits D type Flip-Flop in the unit and choose 8-PSK signal constellation. Normally, we use one bit to select the upper or the lower half-plane, respectively, and two bits select for the four labeled as (00,01,10,11). It can be reduced hardware complexity and the circuits of the a preload unit are get by 5 of 1-bits D type Flip-Flop.

(II). MAP Unit

The input signal of MAP unit is got from the preloader unit. The MAP unit use 5 of one bit Full-Adder. Then, we compare the received bits with preloader bits. So, we obtain the maximum possibility probability through the receiving signals. We have been used the five of 2-bits multiplier and the 5-bits D type Flip-Flop in the circuits to find the maximum possibility probability. Finally, the maximum possible sequence passes 5 bits D type Flip-Flop to get 5 bits binary sequence output. The circuits of MAP decoder unit are get by 4 of MAP unit and a preloader unit.

The implementation circuits of connection with the TTCM and Space-Time code modulation are shown in Fig.3. We issue of concatenation the TTCM and Space-Time code modulation in beyond section. Then, we get the decoder algorithm in MAP unit. In the CODEC, we use 5 bits D type Flip-Flop to simulate channel. Finally, we get the most possible state and good performance from the channel of CODEC at the decoder of output state.

4. Simulation Results

In this paper, we simulate with Altera MAX-PLUS II 9.1 and choose the chip NO: EPF10K30RC208-3 and the floorplan graphic is shown in Fig.4 which use ▓, ▒, ░ and ▉ to express the cells of columns & rows fasttrack/dedicated input, row fasttrack, column fasttrack and local LAB fan-out only. The encoder/decoder require 466 logic cells. We find the signal-noise-ratio S/N is 0.792dB (p=2) that the value approximate

Shannon's limit BER=0.5. The decoding step is increased such as it can be improved performance.

From Eq(1), we also assume that the receiver signal is a Gaussion distribution. Following the treatment in [6], we may approximately write the BER (bit error rate) for 8-PSK as:

$$\text{BER} \approx Q\left[0.765\sqrt{A^2T/2N_0}\right] \qquad (7)$$

Q[x] is Gaussian integral function defined by

$$\text{Q[x]}=\frac{1}{\sqrt{2\pi}}\int_x^{\infty} e^{-u^2/2}\,du \qquad (8)$$

Figure 5 shows the BER for Rayleigh fading with T_s=10ns, 30ns, 60ns…,etc. As the channel changes during one frame, an additional diversity advantage is obtained by the interleaver between the component codes of the Turbo TCM encoder and the Space-Time block code. Depending the simulation result, we get very good performance target FPGA with two receive antennas can be increased power gain, and an 8 state 8-PSK for the concatenation of TTCM and STBC.

5. Conclusion

We use FPGA as simulation to design CODEC in concatenation TTCM and STBC to improve channel coding generation bits and error correction required decoding transmission speed: besides, it increased coding gain and performance by power without increasing transmitted bandwidth and it by required power. Therefore, TTCM and STBC would be very helpful in high speed and massive data transmission. The Space-Time code concatenation Turbo-TCM compare the Turbo-TCM to increase data rate over wireless channels. The CODEC be combined the Space-Time code and Turbo-TCM without increasing the transmitted power and bandwidth, and then increase data rate so as to improve performance. Finally, we can be used the good of transmitter and receiver devices for wireless communication.

6. Reference

[1] C. Berrou, A. Glavieux, and P. Thitimajshima, "Near Shannon limit error-correcting coding and decoding: Turbo codes(1)" in Proc, IEEE Int. Conf. on Communications, Geneva. Switzerland. May 23-26, pp.1064-1070., 1993.

[2] A. Stefanov and T.M. Duman, "Turbo coded modulation for systems with transmit and receive antenna diversity", GOLBECOM'99, pp.2336-2340, Vol.5., 1999.

[3] E.W. Bruce and Y.M. Calvin, "Turbo coding applied to pragmatic trellis-coded Modulation", IEEE, Communications letters. Vol.4., No2, Feb. 2000.

[4] R. Gozali and B.D. Woerner, ”Applying the Calderbank-Mazo algorithm to space-time trellis coding”, Southeastcon 2000. Proc. IEEE, pp309-314., 2000.

[5] A.R. Hammons and H.E. Gamal, ”On the theory of space-time codes for PSK modulation”, IEEE Trans. on Inform. Theory, pp.524-542., Vol.462., Mar. 2000.

[6] A.F. Naguib, V. Tarokh, N. Seahadri and A.R. Calderbank, ”Space-time coded modulation for high data rate wireless communications”, IEEE GLOBECOM’97., pp.102-109, Vol.1., 1997.

[7] G. Bauch and A.F. Naguib, ”MAP equalization of space-time coded signals over frequency selective channel”, IEEE WCNC.’99, pp.261-265, Vol.1, 1999.

[8] Ye Liu, Shu Lin and P.C. Marc, ”MAP algorithm for decoding linear block codes based on sectionalized trellis diagrams”, IEEE Trans. on Commun., pp.577-587., Vol.48., No.4, Apr. 2000.

[9] N. Seshadri, V. Tarokh and A.R. Calderbank, ”Space-time codes for wireless communication: code construction”, Vehicular Technology Conference, 1997, IEEE, 47th, pp.637-641., Vol.2., 1997.

[10] B. Gerhard, “Concatenation of Space-Time block codes and “Turbo”-TCM”, Communications, 1999. ICC’99. 1999 IEEE International Conference on, 1999, pages:1202-1206., Vol.2., 1999.

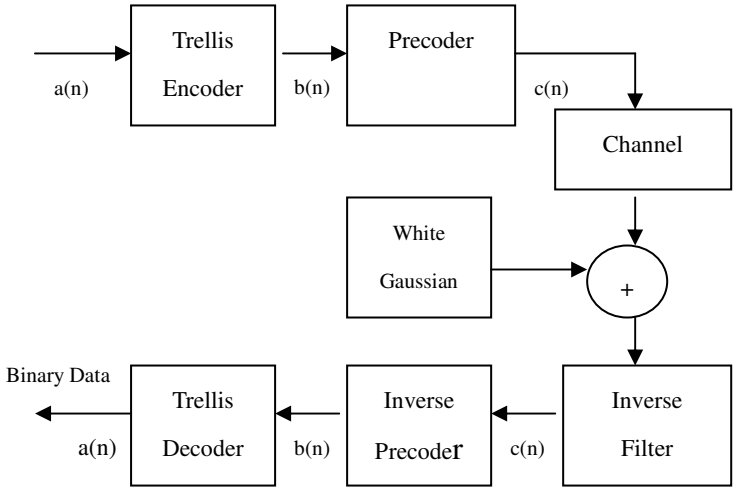

Fig1 Block diagram of combined TCM and precoder

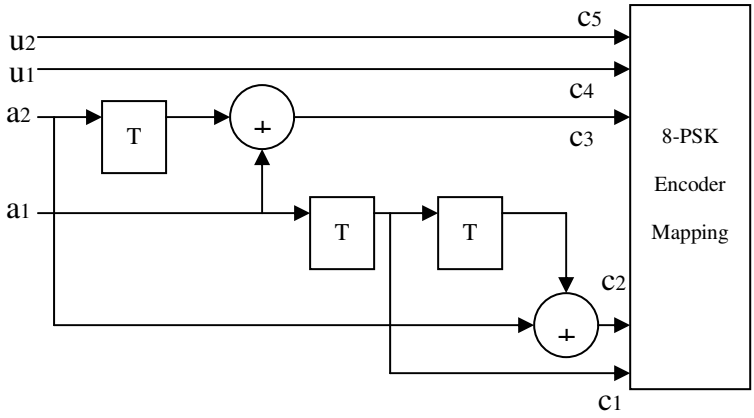

Fig2 8-PSK feedback-free Convolutional encoder 8-state 2/3 Rate

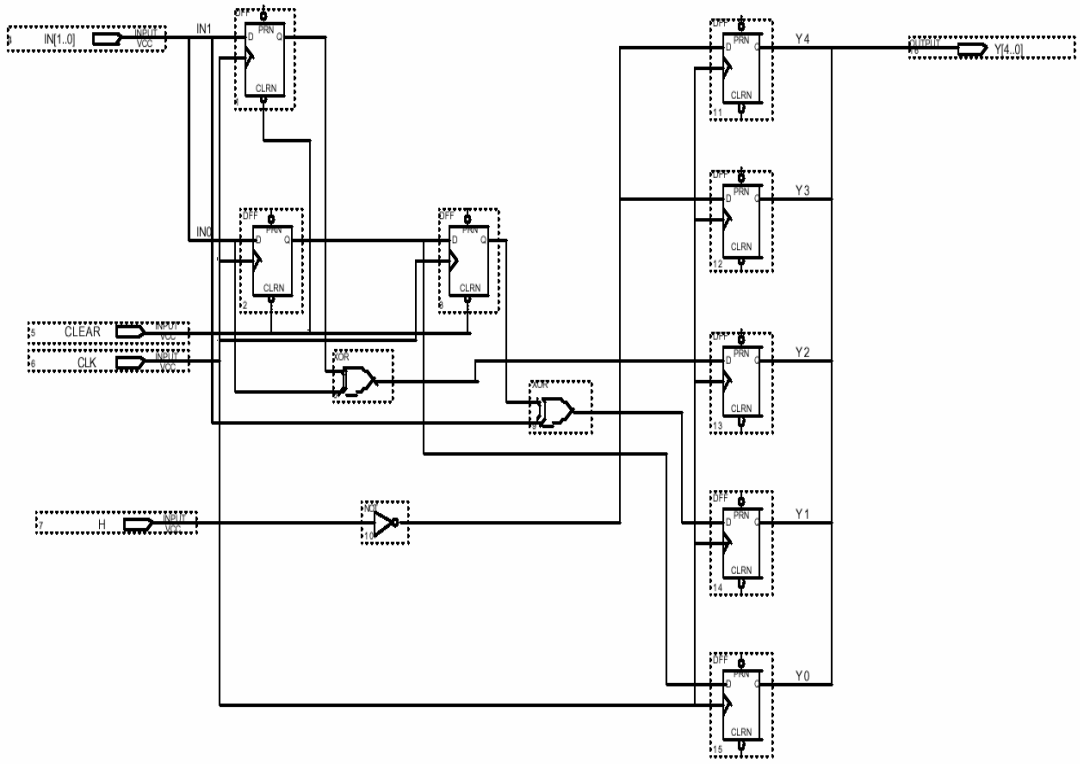

Fig 3 Circuit diagram of trellis encoder unit for 8-PSK

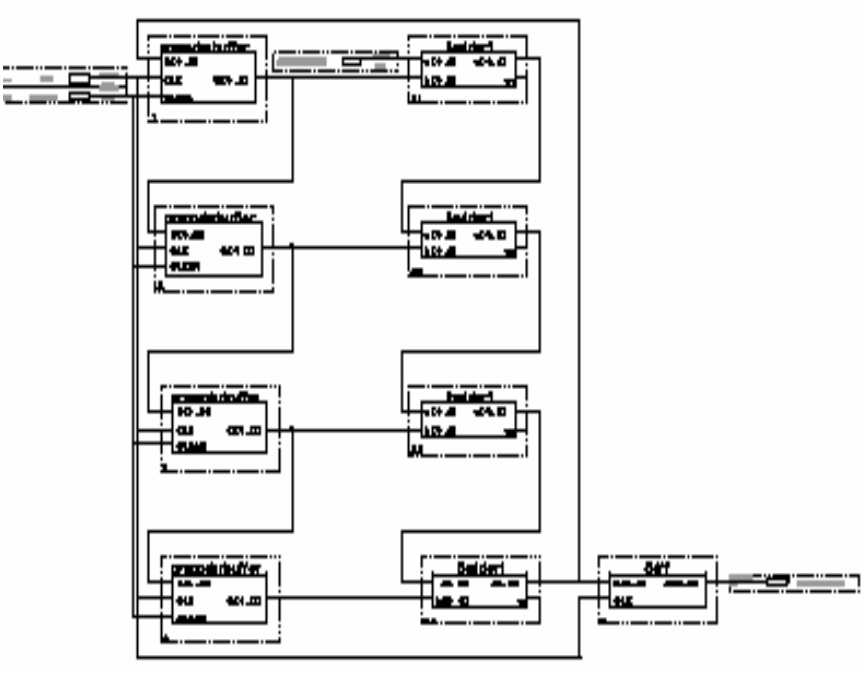

Fig4 Circuit diagram of precoder unit

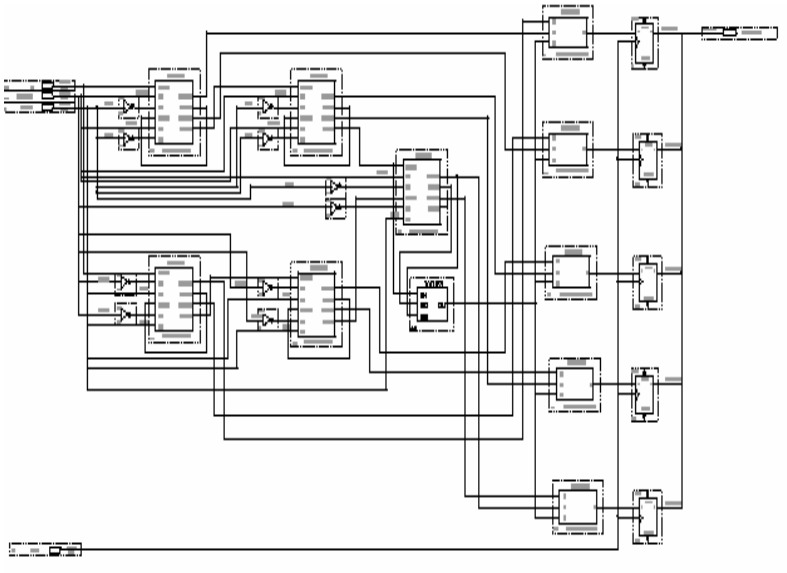

Fig5 Circuit diagram of one unit branch metric calculation

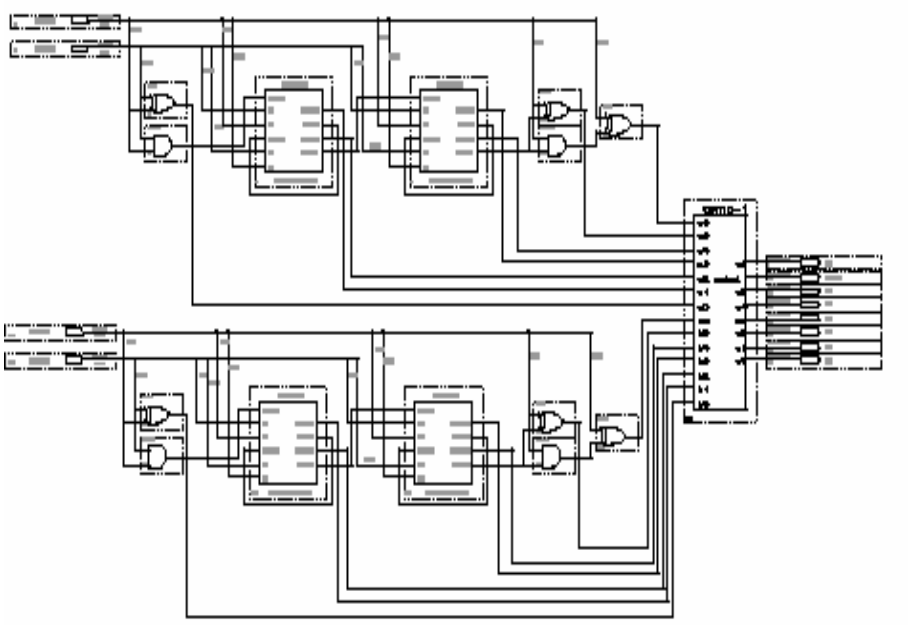

Fig6　Circuit diagram of one unit 2-way ACSU

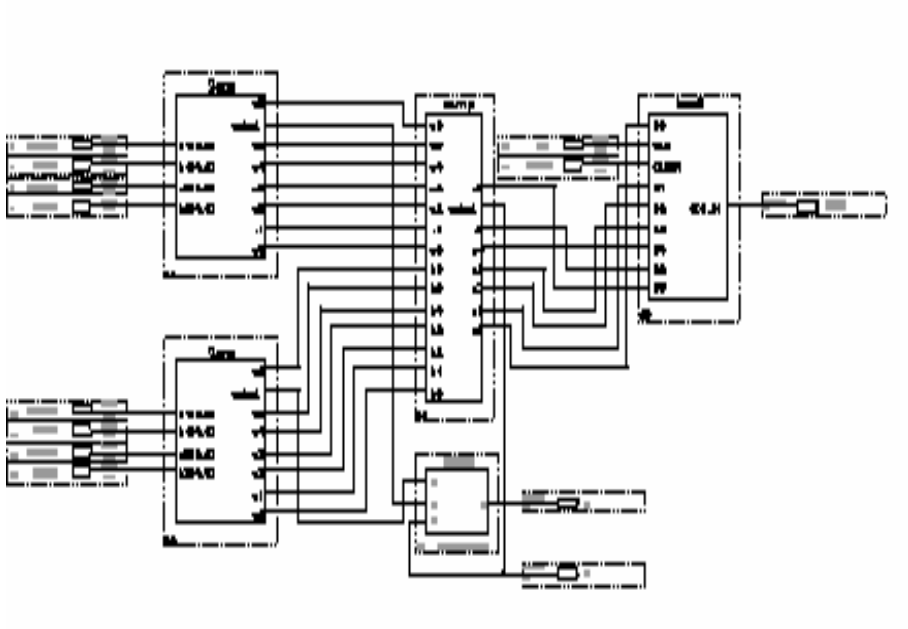

Fig7 Circuit diagram of one unit 4-way Add-Compare-Select

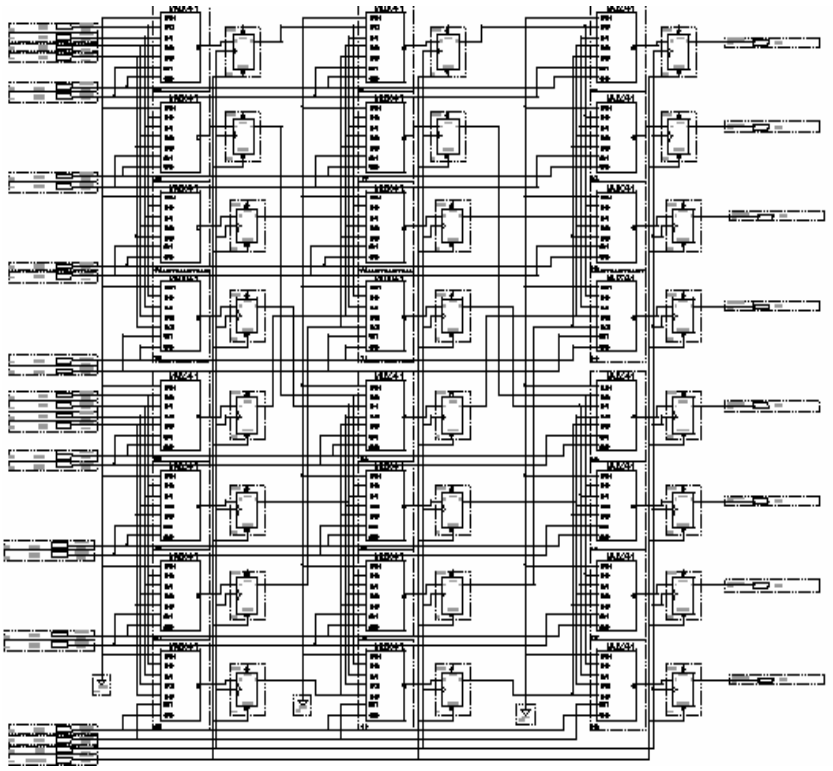

Fig8 Circuit diagram of one unit survivor metric

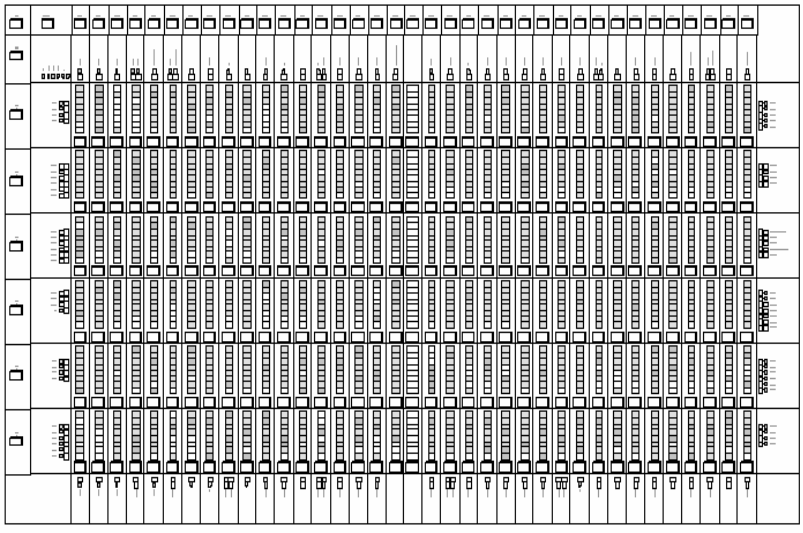

Fig9 The CODEC of floorplan circuit

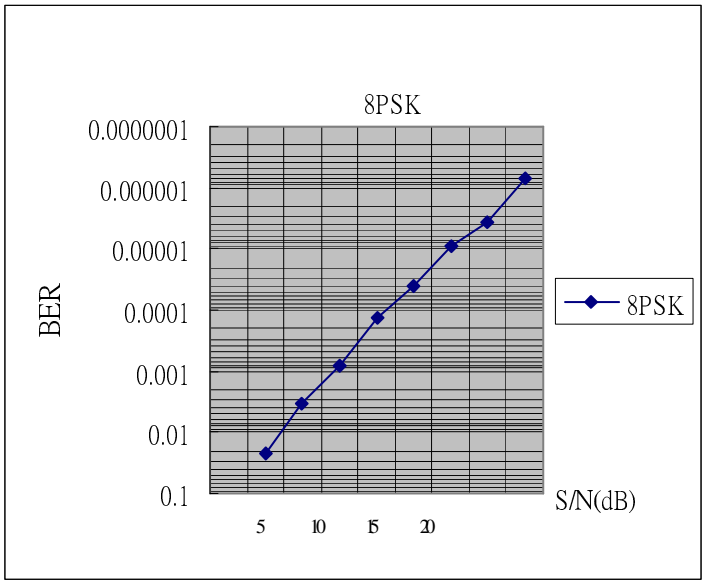

Fig10 The CODEC 8PSK 8states 2/3 rate convolution code in ISI channel

Biography

Jen-Chi Huang was born in Kaohsiung, Taiwan, R.O.C., in 1967. He received the M.S. degree in C.C. from NKFUST(National Kaohsiung First University of Science and Technology), in 1999 and 2001, and is now a Ph.D. candidate at the same university. His research interests are in digital communication and FPGA design.